WHAT IS CLAIMED IS:

1. An optoelectronic transceiver, comprising:

a laser transmitter

a photodiode receiver; and

a controller;

wherein the controller comprises:

memory, including one or more memory arrays for storing information related to the transceiver;

analog to digital conversion circuitry for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory;

an interface for allowing a host to read directly from and write directly to locations within the memory; and

comparison logic for comparing the digital values with limit values to generate flag values, wherein the flag values are stored in predefined locations within the memory during operation of the optoelectronic transceiver.

2. The optoelectronic transceiver of claim 1, further including:

a cumulative clock for generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable via the interface.

3. The optoelectronic transceiver of claim 1, further including:

a cumulative clock for generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is stored comprises one of the memory arrays of the memory.

4. The optoelectronic transceiver of claim 1, further including:

a power supply voltage sensor coupled to the analog to digital conversion circuitry, the power supply voltage sensor generating a power level signal corresponding to a power supply voltage level of the transceiver, wherein the analog to digital conversion circuitry is

configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory.

5. The optoelectronic transceiver of claim 4, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

6. The optoelectronic transceiver of claim 5, wherein

the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory; and

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

7. The optoelectronic transceiver of claim 4, wherein

the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

8. The optoelectronic transceiver of claim 1, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

9. The optoelectronic transceiver of claim 8, wherein

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

10. The optoelectronic transceiver of claim 1, further including

fault handling logic, coupled to the transceiver for receiving at least one fault signal from the transceiver, coupled to the memory to receive at least one flag value stored in the memory, and coupled to a host interface to transmit a computed fault signal, the fault handling logic including computational logic for logically combining the at least one fault signal received from the transceiver and the at least one flag value received from the memory to generate the computed fault signal.

11. The optoelectronic transceiver of claim 1, further including

control adjustment circuitry for adjusting a first control signal of the control signals generated by the control circuitry in accordance with an adjustment value stored in the memory.

12. The optoelectronic transceiver of claim 1, wherein the control circuitry generates the first control signal in accordance with a temperature.

13. The optoelectronic transceiver of claim 1, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

14. An optoelectronic transceiver, comprising:

a laser transmitter;

a photodiode receiver; and

a controller;

wherein the controller comprises:

memory, including one or more memory arrays for storing information related to the optoelectronic transceiver;

analog to digital conversion circuitry for receiving a plurality of analog signals from the optoelectronic transceiver, the analog signals corresponding to operating conditions

of the optoelectronic transceiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory; and

a memory interface for allowing a host to read directly from and write directly to locations within the memory in accordance with commands received from a host device.

15. The optoelectronic transceiver of claim 14, further including:

a cumulative clock for generating a time value corresponding to cumulative operation time of the optoelectronic transceiver, wherein the generated time value is readable via the memory interface.

16. The optoelectronic transceiver of claim 14, further including:

a cumulative clock for generating and storing in a register a time value corresponding to cumulative operation time of the optoelectronic transceiver, wherein the register in which the time value is stored comprises one of the memory arrays of the memory.

17. The optoelectronic transceiver of claim 14, further including:

a power supply voltage sensor coupled to the analog to digital conversion circuitry, the power supply voltage sensor generating a power level signal corresponding to a power supply voltage level of the optoelectronic transceiver, wherein the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory.

18. The optoelectronic transceiver of claim 17, further including:

comparison logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

19. The optoelectronic transceiver of claim 18, further including

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the optoelectronic transceiver, wherein the analog to digital conversion circuitry is configured to

convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

20. The optoelectronic transceiver of claim 19, wherein

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

21. The optoelectronic transceiver of claim 14, further including

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the optoelectronic transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

22. The optoelectronic transceiver of claim 21, further including

comparison logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

23. The optoelectronic transceiver of claim 14, further including

fault handling logic, coupled to the optoelectronic transceiver for receiving at least one fault signal from the optoelectronic transceiver, coupled to the memory to receive at least one flag value stored in the memory, and coupled to a host interface to transmit a computed fault signal, the fault handling logic including computational logic for logically combining the at least one fault signal received from the optoelectronic transceiver and the at least one flag value received from the memory to generate the computed fault signal.

24. The optoelectronic transceiver of claim 14, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

25. An optoelectronic transceiver, comprising:

a laser transmitter;

a photodiode receiver; and

a controller;

wherein the controller comprises:

analog to digital conversion circuitry for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined memory mapped locations within the integrated circuit;

comparison logic for comparing the digital values with limit values to generate flag values, wherein the flag values are stored in predefined memory mapped locations within the integrated circuit during operation of the optoelectronic transceiver;

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the integrated circuit; and

a memory mapped interface for allowing a host to read directly from and write directly to locations within the integrated circuit and for accessing memory mapped locations within the integrated circuit for controlling operation of the control circuitry.

26. An optoelectronic transceiver, comprising:

a laser transmitter;

a photodiode receiver; and

a controller;

wherein the controller comprises:

memory, including one or more memory arrays for storing information related to the optoelectronic transceiver;

analog to digital conversion circuitry configured to receive a plurality of analog signals, the analog signals corresponding to operating conditions of the optoelectronic transceiver, converting at least one of the received analog signals into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory; and

a memory interface for allowing a host device to read directly from and write directly to locations within the memory in accordance with commands received from a host device.

27. The optoelectronic transceiver of claim 26, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in the at least one predefined location within the memory.

28. The optoelectronic transceiver of claim 26, wherein the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the controller, wherein the analog to digital conversion circuitry is configured to convert the voltage signal into a digital voltage value and to store the digital voltage value in the at least one predefined location within the memory.

29. An optoelectronic transceiver, comprising:

a laser transmitter;

a photodiode receiver; and

a controller;

wherein the controller comprises:

memory, including one or more memory arrays for storing information related to the optoelectronic transceiver;

analog to digital conversion circuitry for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic transceiver, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory; and

a memory interface for allowing a host device to read directly from and write directly to locations within the memory in accordance with commands received from a host device.

30. The optoelectronic transceiver of claim 29, further including:

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in the at least one predefined location within the memory.

31. The optoelectronic transceiver of claim 30, further including control circuitry, responsive to the digital temperature value for controlling operation of the optoelectronic transceiver.

32. The optoelectronic transceiver of claim 29, wherein the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the controller, wherein the analog to digital conversion circuitry is configured to convert the voltage signal into a digital voltage value and to store the digital voltage value in the at least one predefined location within the memory.

33. The optoelectronic transceiver of claim 29, further including control circuitry, responsive to the at least one digital value for controlling operation of the optoelectronic transceiver.